SRM Institute o

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**SRM College of Engineering and Technology**

**School of Computing**

**DEPARTMENT OF COMPUTING TECHNOLOGIES**

SRM Nagar, Kattankulathur – 603203, Chengalpattu District, Tamilnadu

**Academic Year: 2022-2023**

**MCQ ANSWER KEY**

**Test: CLAT-1 Date: 12-9-2022**

**Course Code & Title: 18CSC203J: Computer Organization and Architecture Duration: 1 Period**

**Year & Sem: II & III Max. Marks: 25 Marks**

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| Course Outcomes (CO): | | | | | | *The learners will be able to attain CO1* | | | | | | | | | |
| **CO-1 :** | | *Identify the computer hardware and how software interacts with computer hardware* | | | | | | | | | | | | | |
| Program Outcomes (PO) | | | | | | | | | | | | |  | | |
| 1 | 2 | 3 | 4 | 5 | 6 | | 7 | 8 | 9 | 10 | 11 | 12 | PSO | | |
| Engineering Knowledge | Problem Analysis | Design & Development | Analysis, Design, Research | Modern Tool Usage | Society & Culture | | Environment & Sustainability | Ethics | Individual & Team Work | Communication | Project Mgt. & Finance | Life Long Learning | PSO - 1 | PSO - 2 | PSO – 3 |
| *3* | *3* |  |  |  |  | |  |  | *2* | *1* |  | *2* |  |  | |

3-High, 2- Medium, 1-low

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| **Part – A**  **(15 x 1 = 15 Marks) Instructions: Answer all** | | | | | | |
| **Q. No** | **Question** | **Marks** | **BL** | **CO** | **PO** | **PI Code** |
| **1** | Which of the following is at the lowest level in the memory hierarchy?  Cache Memory  Secondary memory  Registers  RAM  **ANSWER: Secondary Memory** | **1** | **1** | **1** | **1** | **1.6.1** |
| **2** | Consider a 32- bit processor, the address of the contents are 1000, 1004, 1008, and 1012. Now MAR holds an address namely 1000 to fetch the content from the memory. What is the content of the program counter (PC)?  1000  1004  1008  1012  **ANSWER: 1004** | **1** | **3** | **1** | **2** | **2.8.1** |
| **3** | The instructions which copy information from one location to another either in the processor’s internal register set or in the external main memory are called \_\_\_\_\_\_  Data transfer instructions  Program control instructions  Input-Output instructions  Logical Instructions  **ANSWER: Data transfer instructions** | **1** | **1** | **1** | **1** | **1.6.1** |
| **4** | Perform the Right Rotation by shifting 3 bits for the following bits:11100101  01110010  00101111  11001011  10111100  **ANSWER: 10111100** | **1** | **3** | **1** | **1** | **1.2.1** |
| **5** | In which addressing mode the instruction contains explicit operand?  Absolute  Immediate  Indirect  Direct  **ANSWER : Immediate** | **1** | **1** | **1** | **1** | **1.6.1** |
| **6** | A stack-organized computer has  Three-address instruction  Two-address instruction  One-address instruction  Zero-address instruction  **ANSWER: Zero-address instruction** | **1** | **2** | **1** | **1** | **1.6.1** |
| **7** | Perform binary subtraction: 101111 – 010101  100100  010101  011010  011001  **ANSWER: 011010** | **1** | **3** | **1** | **1** | **1.6.1** |
| **8** | The instruction -> Add LOCA, R0 \_\_\_\_\_\_\_  adds the value of LOCA to R0 and stores in the temp register  adds the value of R0 to the address of LOCA  adds the values of both LOCA and R0 and stores it in R0  adds the value of LOCA with a value in accumulator and stores it in R0  **ANSWER: adds the values of both LOCA and R0 and stores it in R0** | **1** | **3** | **1** | **1** | **1.7.1** |
| **9** | The instruction, Add Loc, R1 in Register Transfer Notation [RTN] is \_\_\_\_\_\_\_  AddSetCC Loc+R1  R1=Loc+R1  Not possible to write in Register Transfer Notation [RTN]  R1<-[Loc]+[R1]  **ANSWER: R1<-[Loc]+[R1]** | **1** | **3** | **1** | **2** | **2.6.2** |
| **10** | The Instruction fetch phase ends with \_\_\_\_\_\_\_\_\_  Placing the data from the address in MAR into MDR  Placing the address of the data into MAR  Completing the execution of instructions and placing the storage  address into MAR  Decoding the data in MDR and placing it in IR  **ANSWER: Decoding the data in MDR and placing it in IR** | **1** | **1** | **1** | **1** | **1.6.1** |
| **11** | **(2FAOC) 16 is equivalent to**  (195084)10  (00101111101000001100)2  (194 085)10  (00101111101000001101)2  **ANSWER: (00101111101000001100)2** | **1** | **3** | **1** | **1** | **1.6.1** |
| **12** | The ALU gives the output of the operations and the output is stored in the \_\_\_\_\_\_\_\_  Memory Devices  Registers  Flags  Output Unit  **ANSWER: Registers** | **1** | **1** | **1** | **1** | **1.6.1** |
| **13** | The binary equivalent of the decimal number 10 is \_\_\_\_\_\_\_\_\_\_  0010  1010  010  **ANSWER: 1010** | **1** | **3** | **1** | **2** | **2.5.2** |
| **14** | **Calculate the 8-bit addition of two operands for 1C+7E**  8C  9B  9A  8D  **ANSWER: 9A** | **1** | **3** | **1** | **1** | **1.6.1** |
| **15** | Which memory unit has the lowest access time?  Cache  Registers  Magnetic Disk  Main Memory  **ANSWER: Registers** | **1** | **2** | **1** | **1** | **1.6.1** |